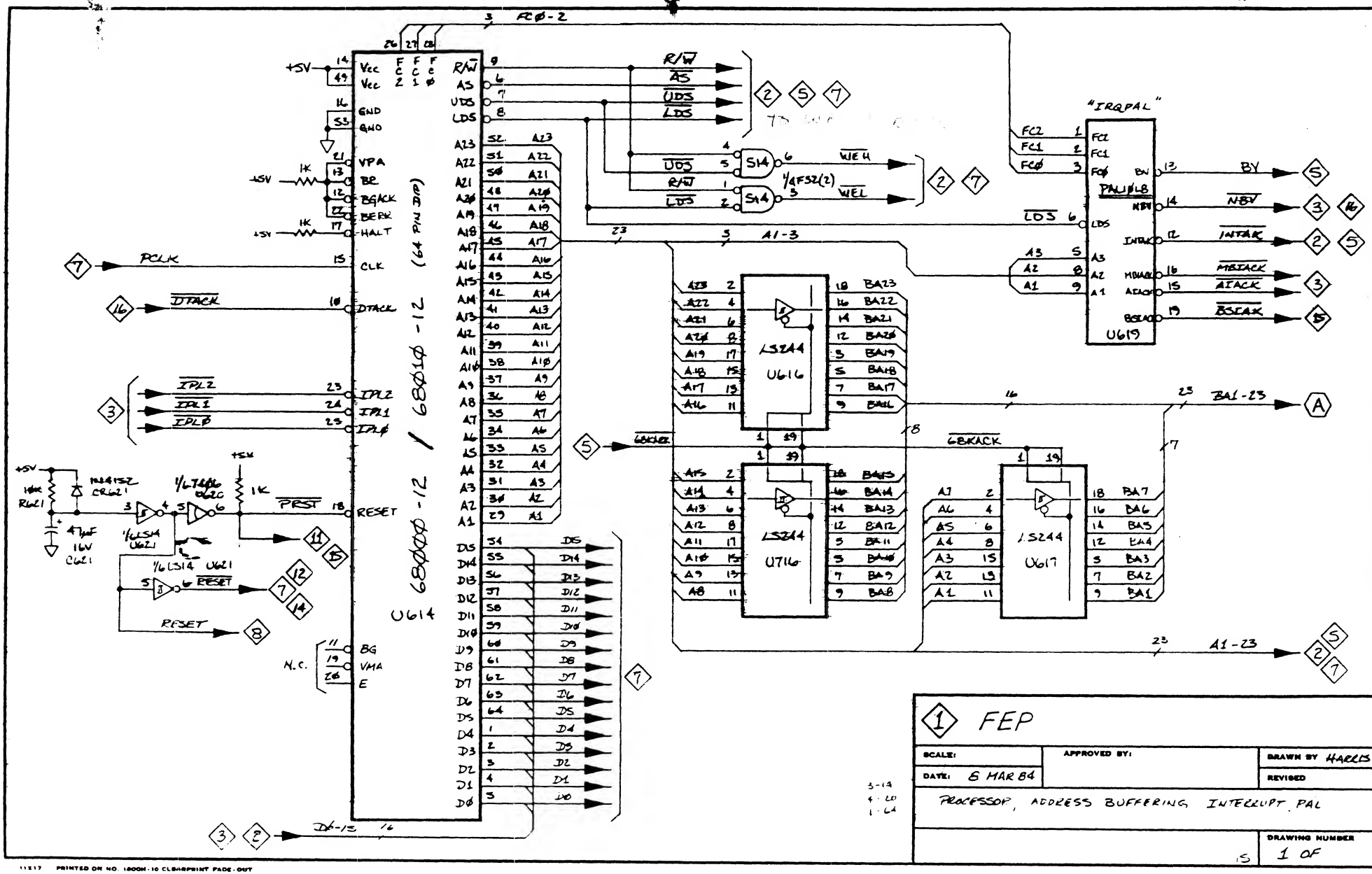
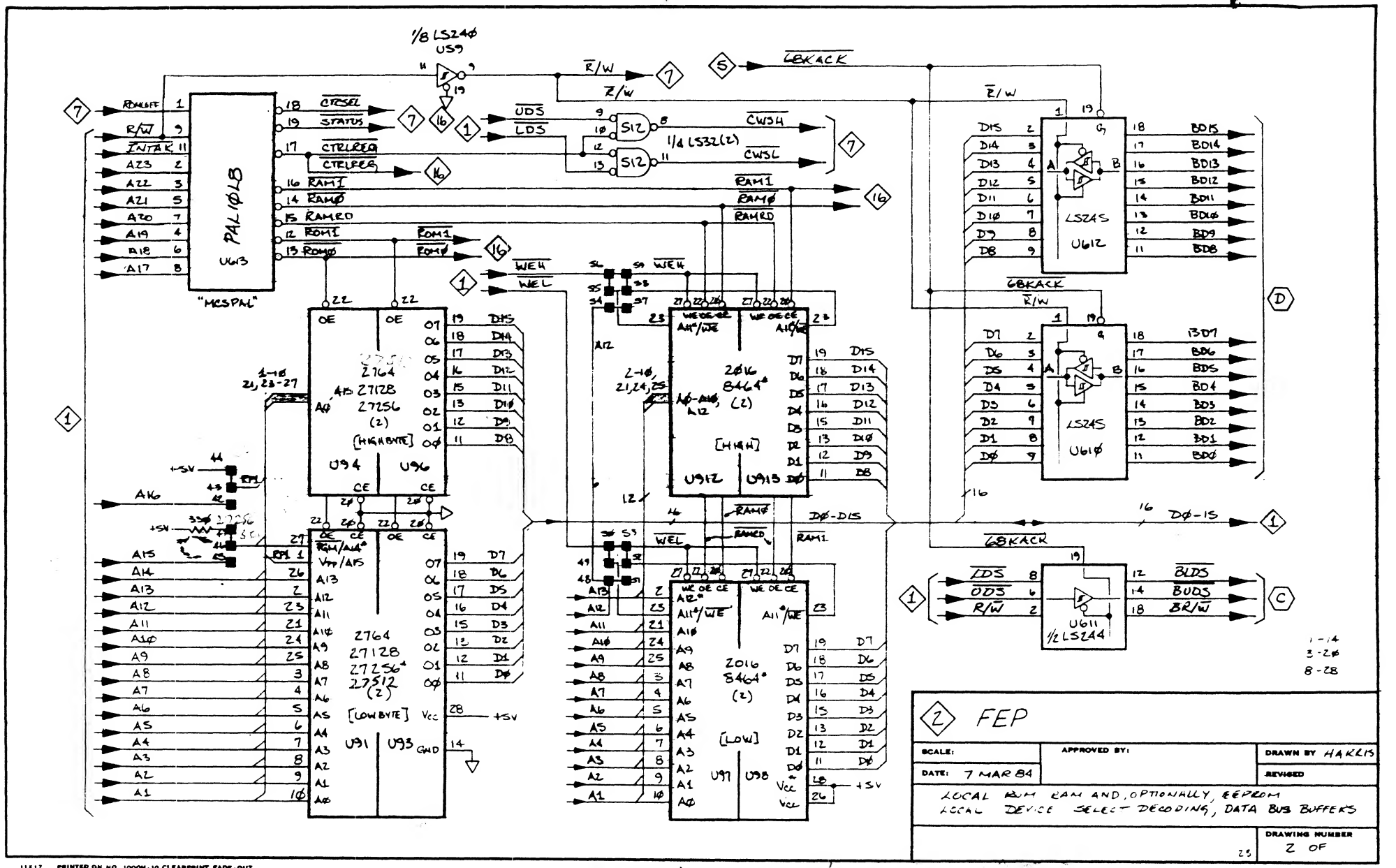
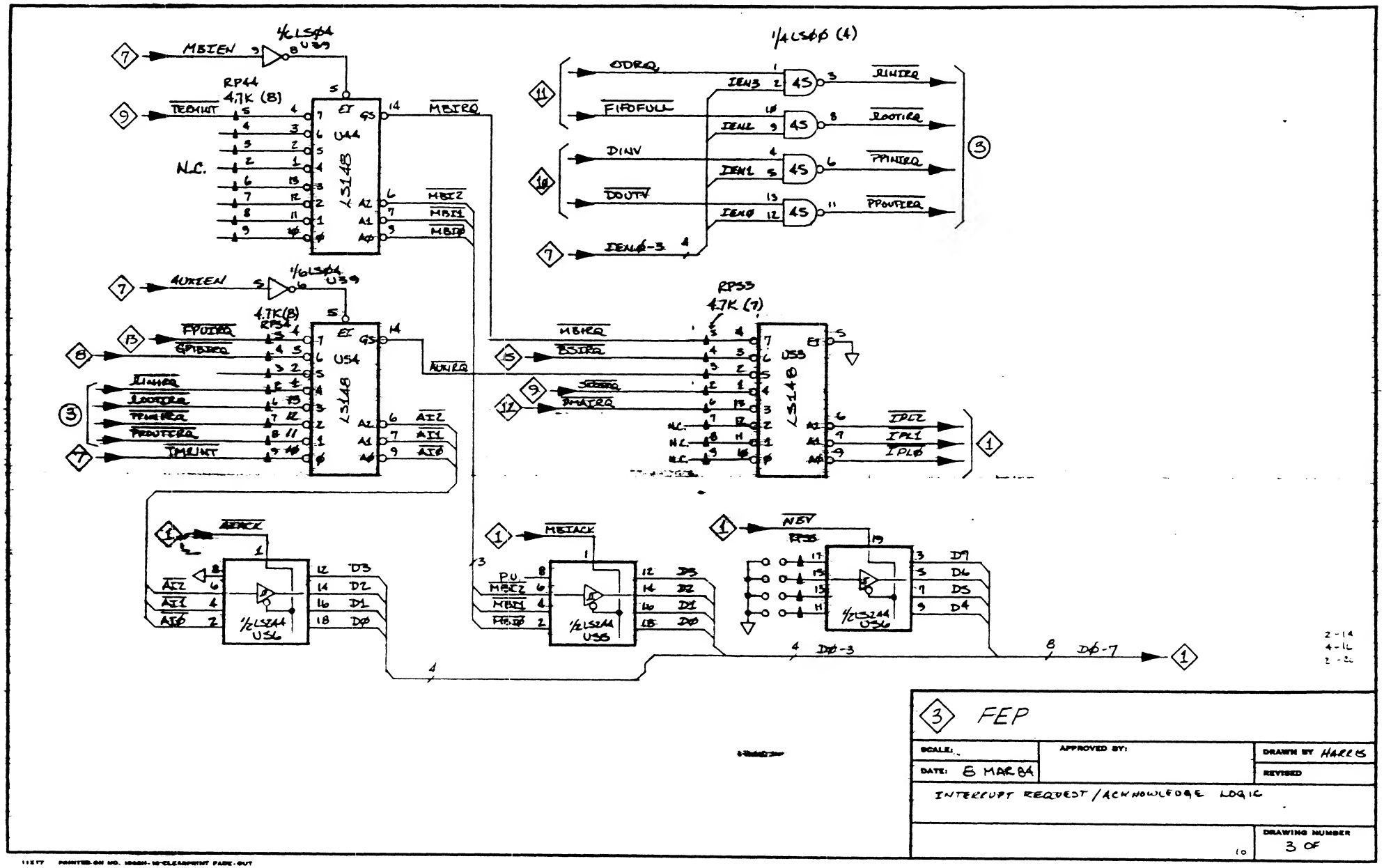




11X17 PRINTED ON NO 1000H-10 CLEARPRINT FADE-OUT

MCSPal

CtrlReg
CtcSel
STATUS



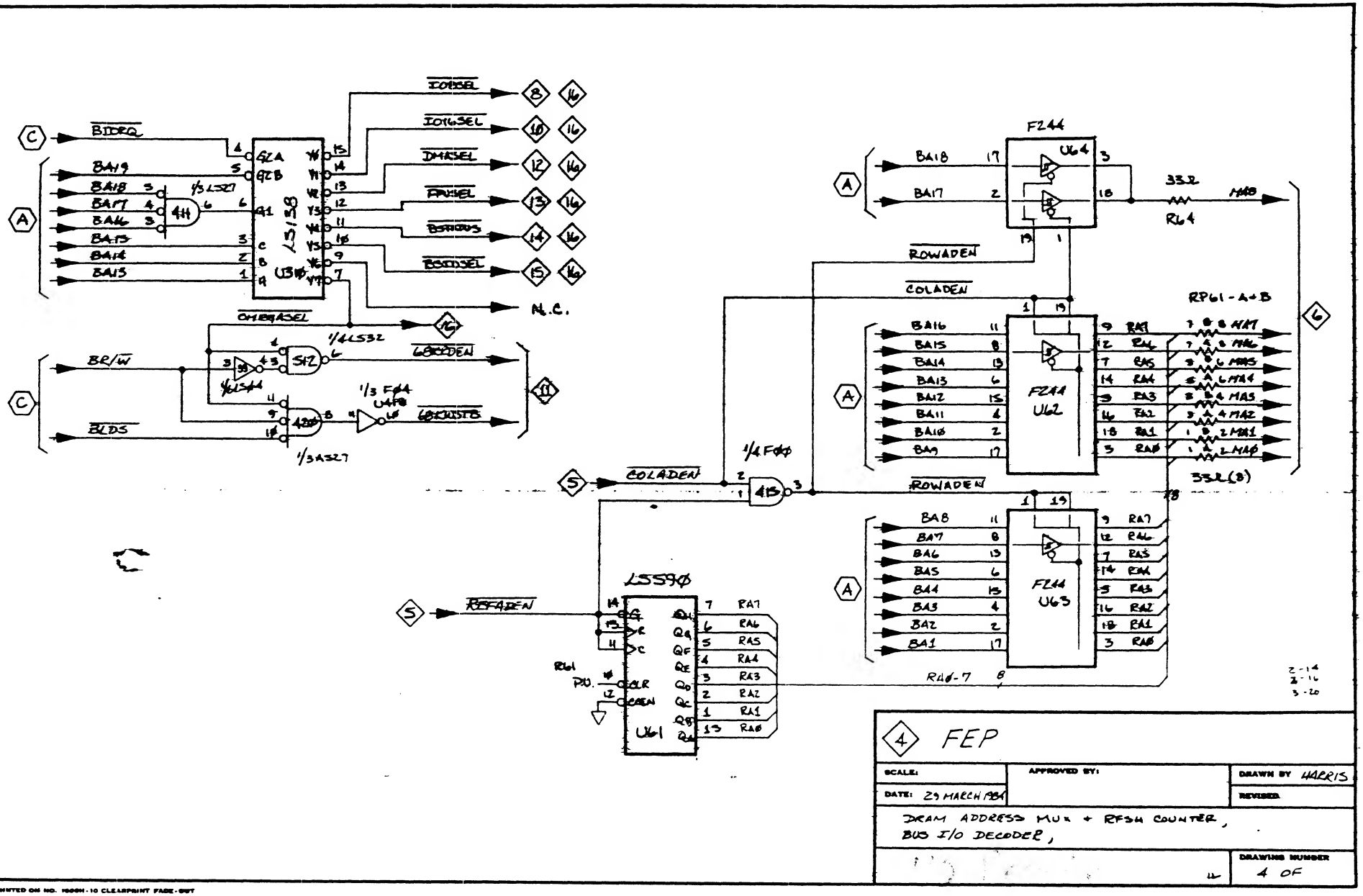
3 FEP

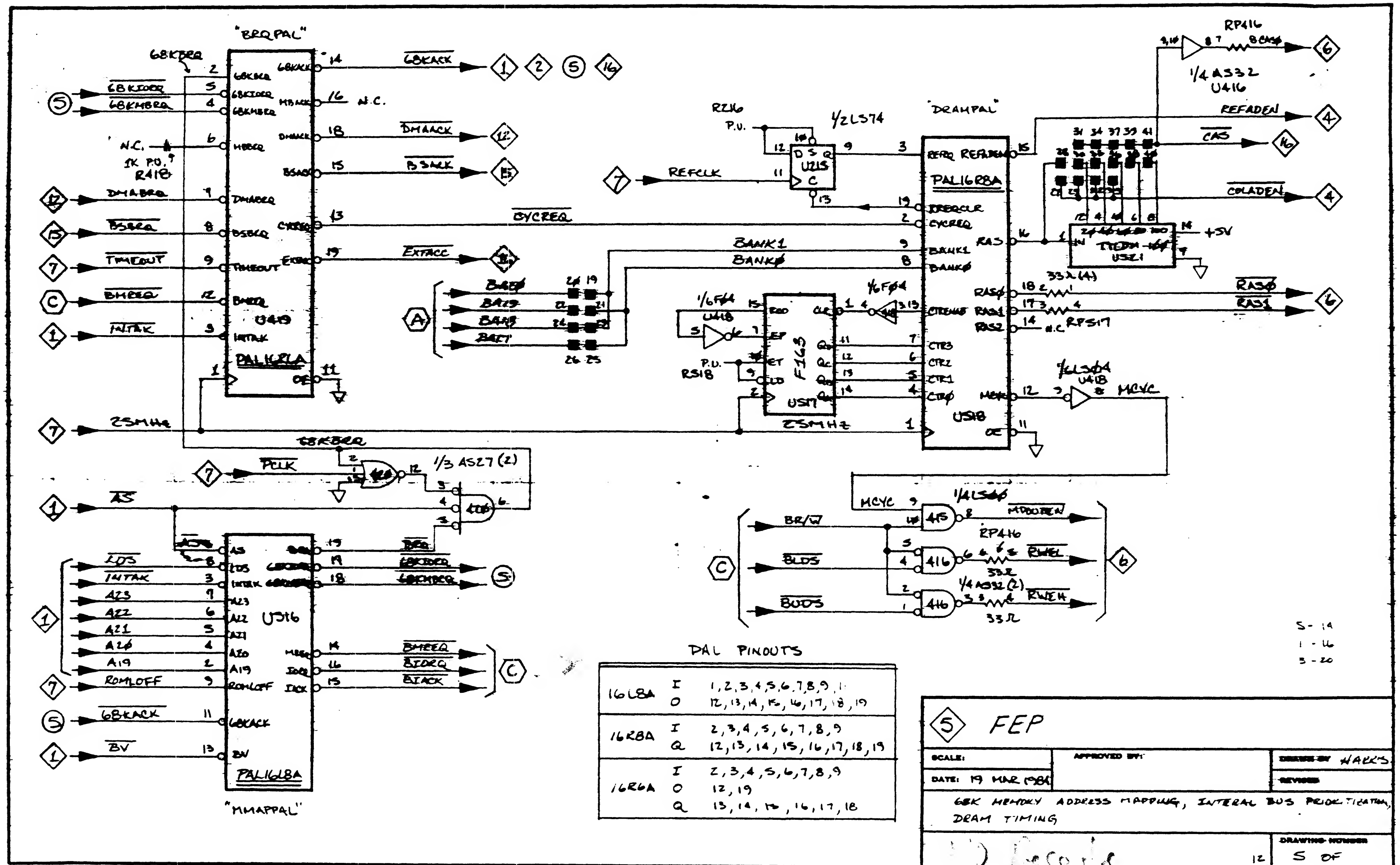
SCALE:	APPROVED BY:	DRAWN BY HARRIS
DATE: 6 MAR 84		REVISED

INTERRUPT REQUEST/ACKNOWLEDGE LOGIC

10

DRAWING NUMBER 3 OF


BIDRQ
BA19
BA18
BA17
BA16
BA15
BA14
BA13
1/3 LS27
LS138
U13
IOBSEL
IOHLSEL
DMASEL
EPUSEL
BSTRDS
BOOTSEL
N.C.
OMBBASEL
1/4 LS32
BR/W
BLDS
1/4 LS04
1/3 F04
U47B
LBOOTEN
LBOOTSTB
1/3 LS27
1/4 F00
COLADEN
ROWADEN
RFSHDEN
LS590
U61
RA7
RA6
RA5
RA4
RA3
RA2
RA1
RA0
RP61
F244
U64
U62
U63
332
RP61-A+B
332(8)
RA6-7
4 FEP
SCALE:
APPROVED BY:
DRAWN BY HARRIS
DATE: 29 MARCH 1984
REVISED
DRAM ADDRESS MUX + RFSH COUNTER,
BUS I/O DECODER,
DRAWING NUMBER
4 OF



DAL PINOUTS

16L8A	I	1, 2, 3, 4, 5, 6, 7, 8, 9, 11
	O	12, 13, 14, 15, 16, 17, 18, 19
16R8A	I	2, 3, 4, 5, 6, 7, 8, 9
	Q	12, 13, 14, 15, 16, 17, 18, 19
16R6A	I	2, 3, 4, 5, 6, 7, 8, 9
	O	12, 19
	Q	13, 14, 15, 16, 17, 18

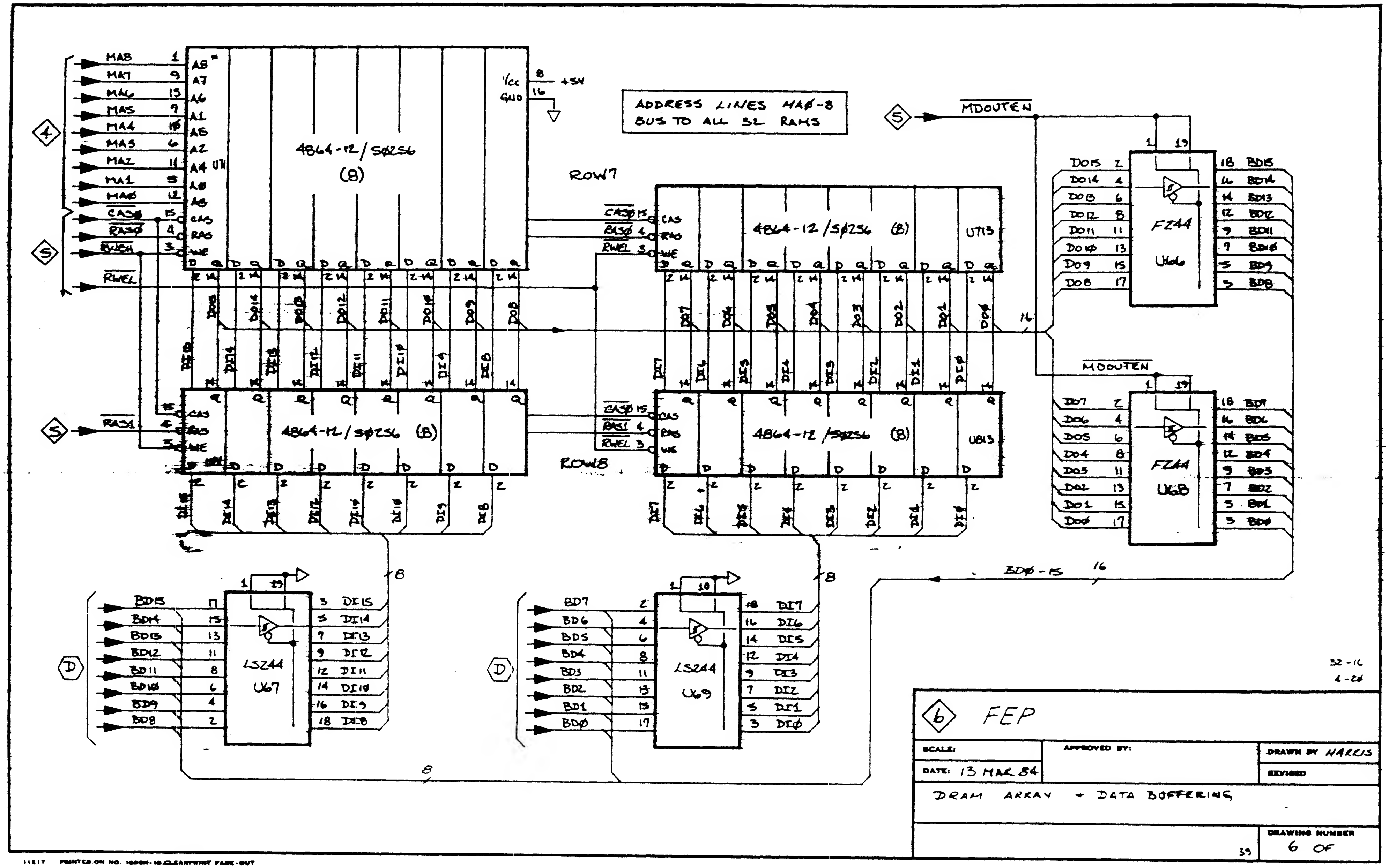
S - 14
I - 16
3 - 20

5 FEP

SCALE:
APPROVED BY:
DRAWN BY HAWKS
DATE: 19 MAR 1984
REVISED

68K MEMORY ADDRESS MAPPING, INTERNAL BUS PRIORITIZATION, DRAM TIMING

DRAWING NUMBER 5 OF 12



FEP

SCALE:

APPROVED BY:

DRAWN BY HARRIS

DATE: 13 MAR 84

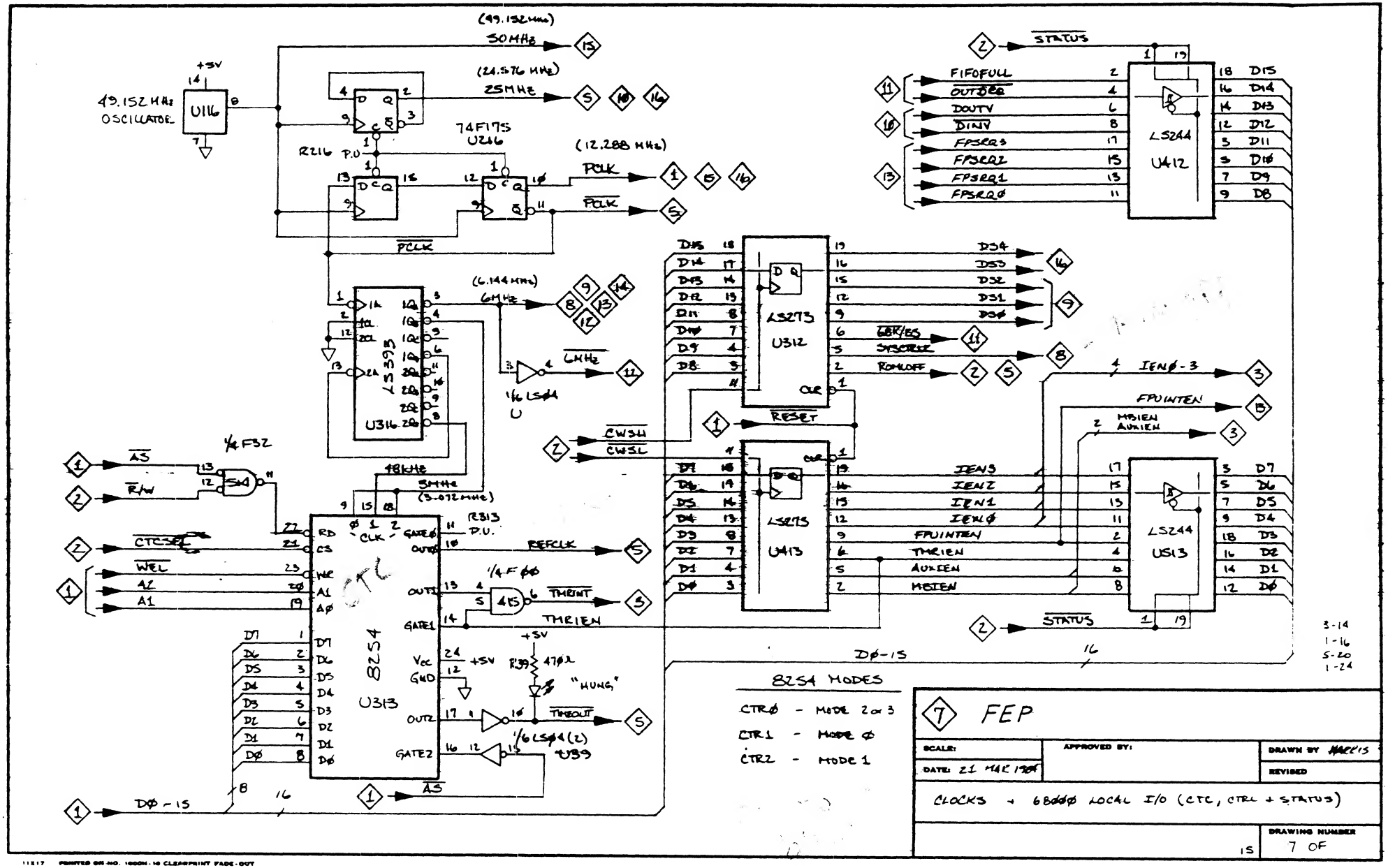
REVISED

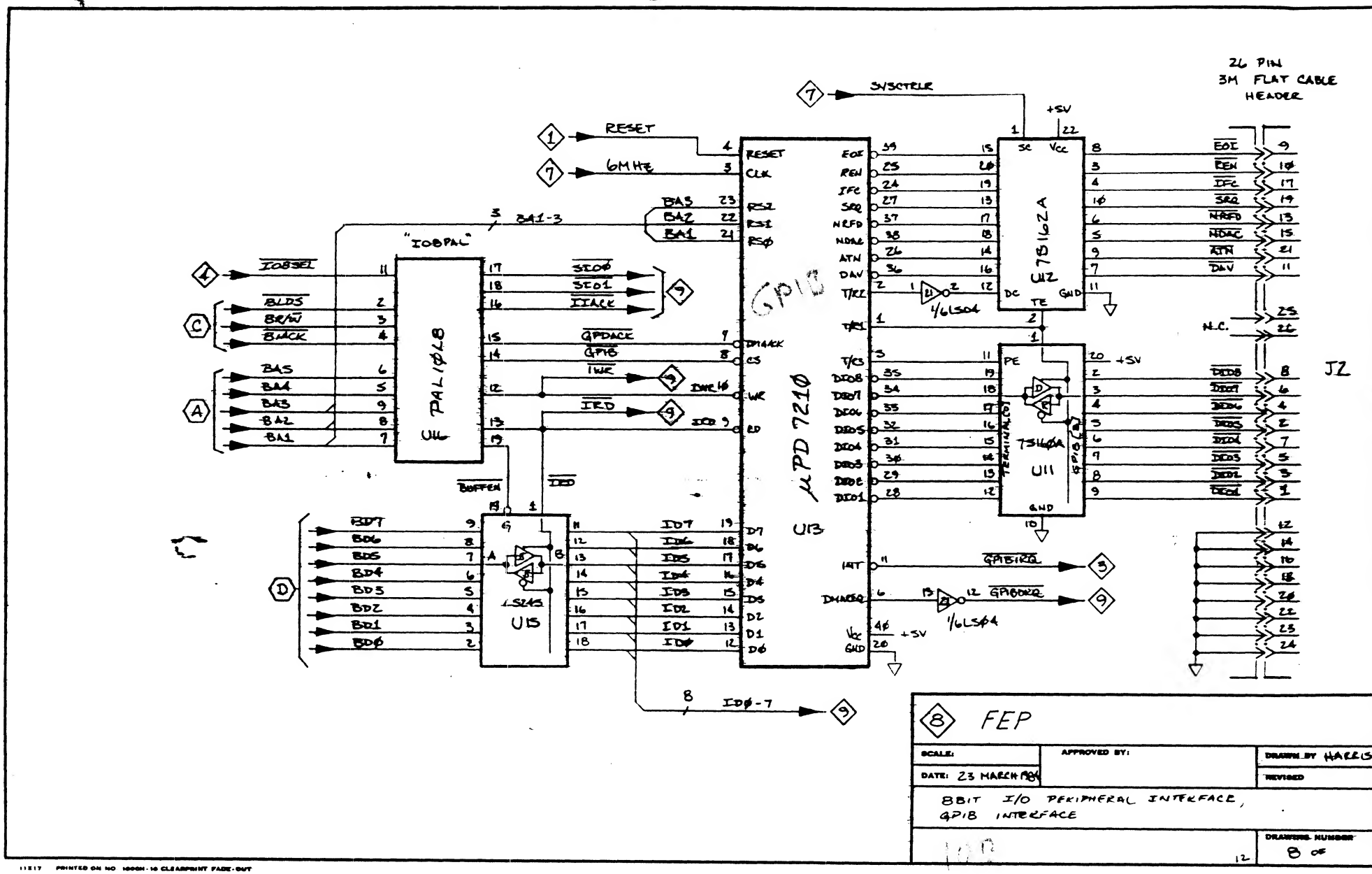
DRAM ARRAY + DATA BUFFERING

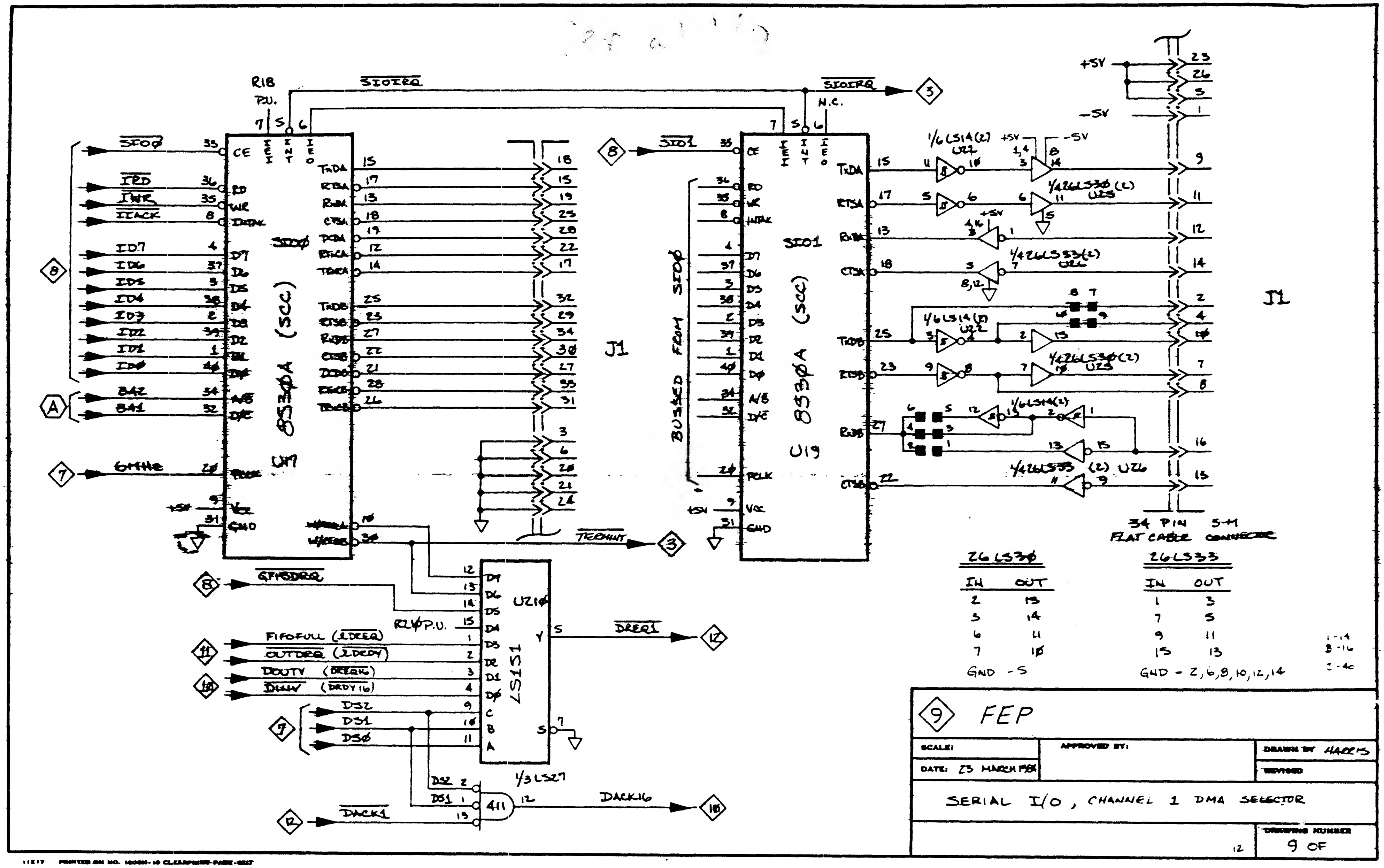
DRAWING NUMBER 6 OF

39

11X17 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT


(49.152MHz)
50MHz
(24.576 MHz)
25MHz
49.152 MHz OSCILLATOR
U116
+5V
74F175
U216
R216 P.U
(12.288 MHz)
PCLK
PCLK
(6.144 MHz)
6MHz
6MHz
1/6 LS04
U
LS393
U316
1/4 F32
A3
R/W
CTCSEL
WEL
A2
A1
18kHz
5MHz
(5.072MHz)
8254
U313
RD
CS
WR
A1
A0
CLK
GATE0
OUT0
OUT1
GATE1
Vcc
GND
OUT2
GATE2
R313
P.U.
REFCLK
1/4 F00
THRINT
THRIEN
R339
470Ω
"HUNG"
THROUT
1/6 LS04(2)
U39
A5
D0-15
8
16
CWSH
CWSL
RESET
LS273
U312
LS273
U413
D5
D4
D3
D2
D1
D0
GBR/BS
SYSCRSR
ROMLOFF
IEN3
IEN2
IEN1
IEN0
FPUINTEN
THRIEN
AUXIEN
MSIEN
STATUS
FIFOFULL
OUTDEB
DOUTV
DINV
FPSRQ3
FPSRQ2
FPSRQ1
FPSRQ0
LS244
U412
LS244
U513
IEN0-3
FPUINTEN
MSIEN
AUXIEN
STATUS
D0-15
8254 MODES
CTR0 - MODE 2 or 3
CTR1 - MODE 0
CTR2 - MODE 1
7 FEP
SCALE:
APPROVED BY:
DRAWN BY MARRIS
DATE: 21 MAR 1984
REVISED
CLOCKS + 68000 LOCAL I/O (CTC, CTRL + STATUS)
DRAWING NUMBER
7 OF
3-14
1-16
5-20
1-24



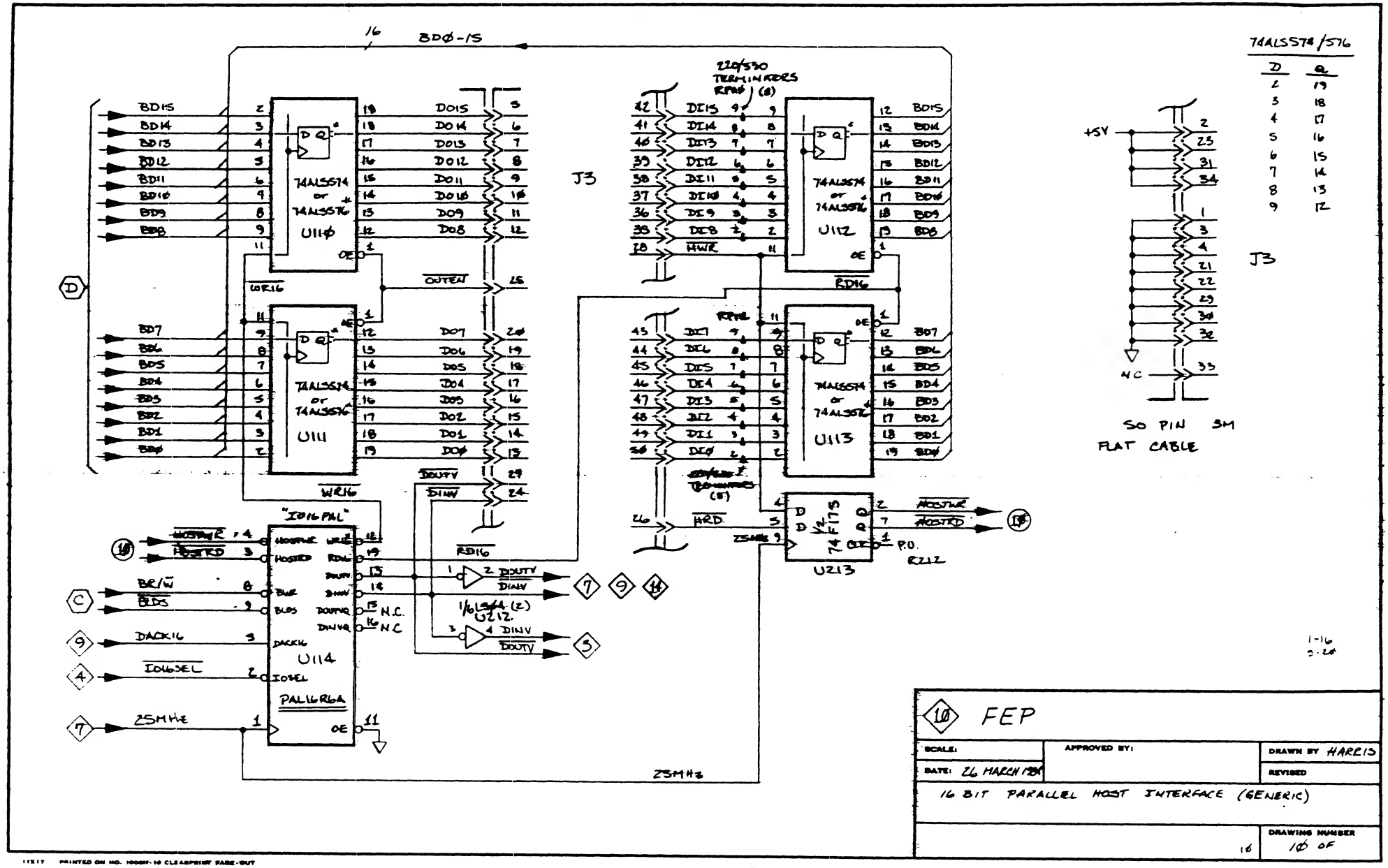


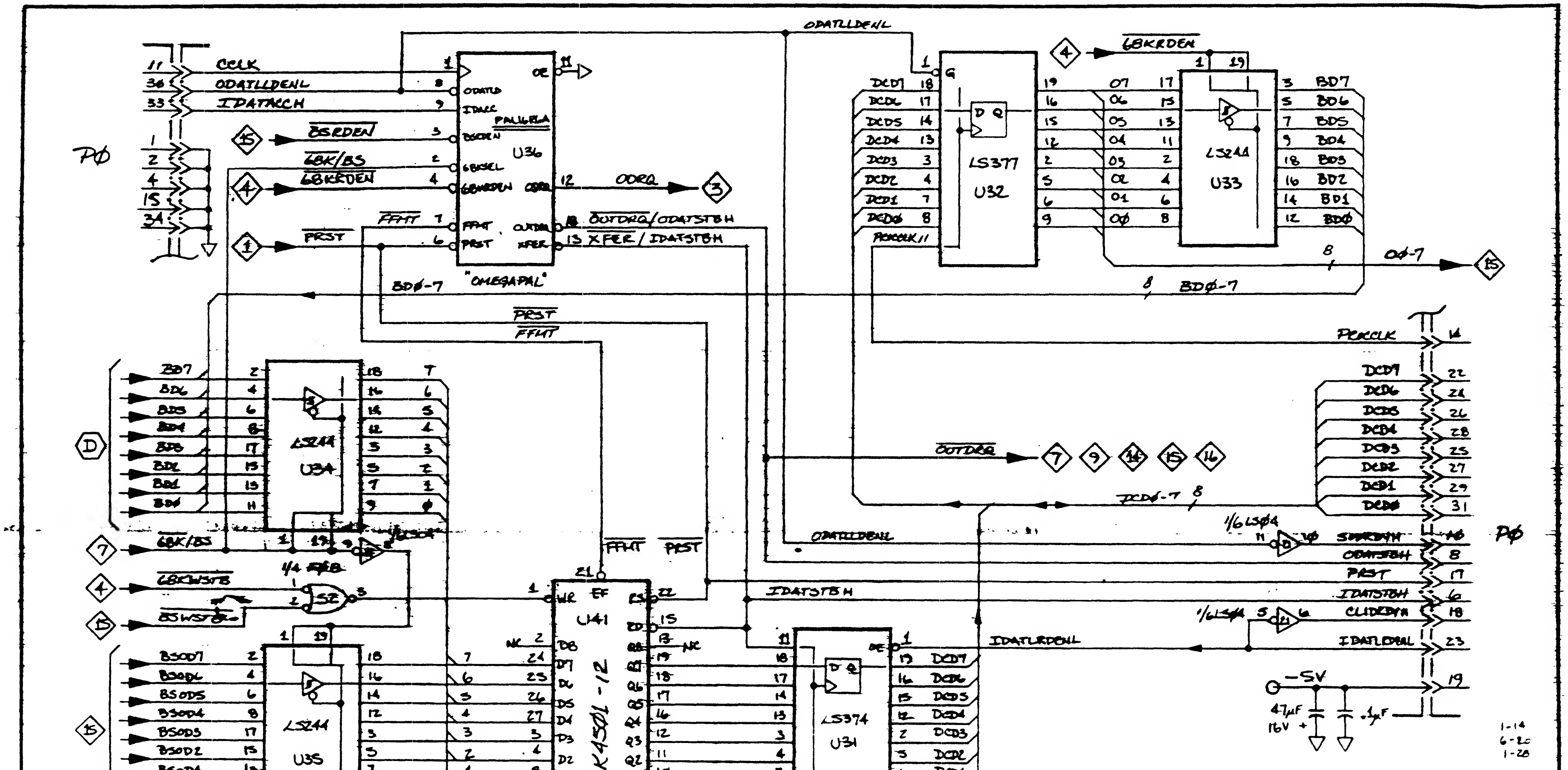
9 FEP

SCALE:
APPROVED BY:
DRAWN BY HARRIS
DATE: 23 MARCH 198?
REVISED

SERIAL I/O, CHANNEL 1 DMA SELECTOR

DRAWING NUMBER 9 OF 12


16
BD0-15
220/330
TERMINATORS
RP#
(8)
J3
74ALS574
or
74ALS576
U110
U111
U112
U113
WR16
RD16
OUTEN
DOUTV
DINV
HRD
HWR
"IO16 PAL"
U114
PAL16R6A
IO16SEL
DACK16
R/W
DS
ZSMHz
U213
74F175
P.D.
R212
HOSTWR
HOSTRD
N.C.
+5V
NC
50 PIN SM
FLAT CABLE
74ALS574/576
D
Q
FEP
SCALE:
APPROVED BY:
DRAWN BY HARRIS
DATE: 26 MARCH 1986
REVISED
16 BIT PARALLEL HOST INTERFACE (GENERIC)
DRAWING NUMBER
10 OF
16



FEP

SCALE:

DATE: 28 MARCH 84

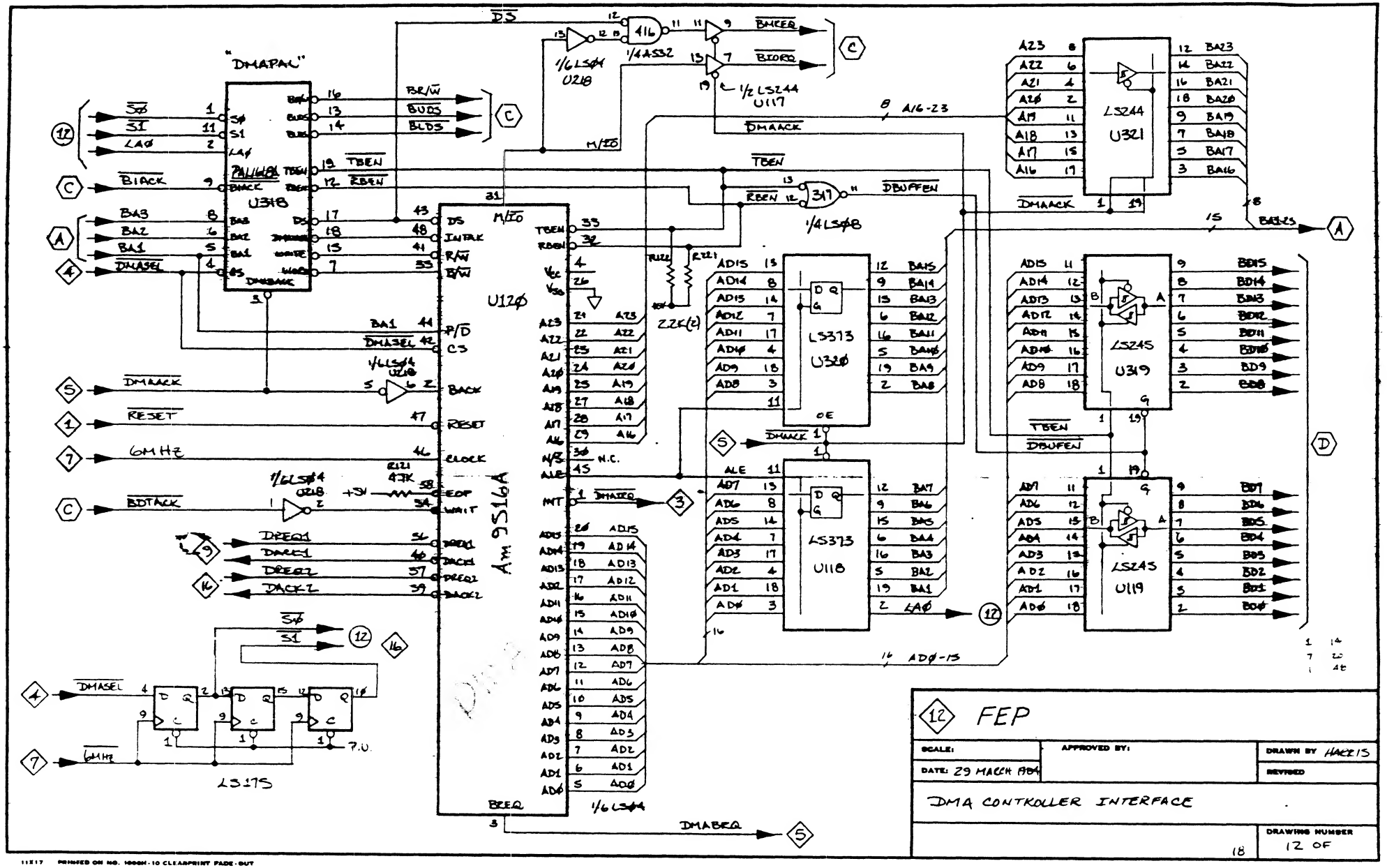
APPROVED BY:

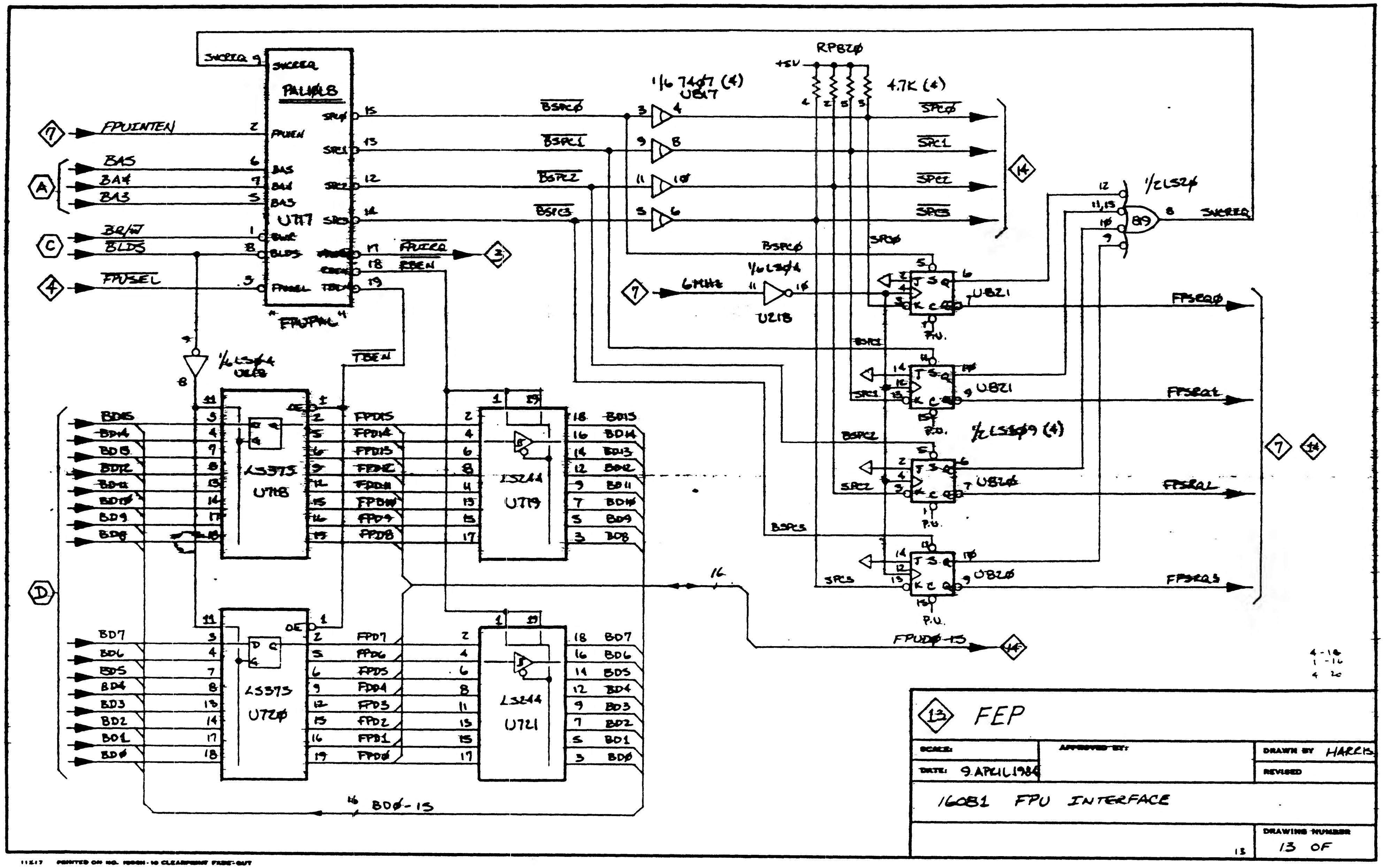
DRAWN BY

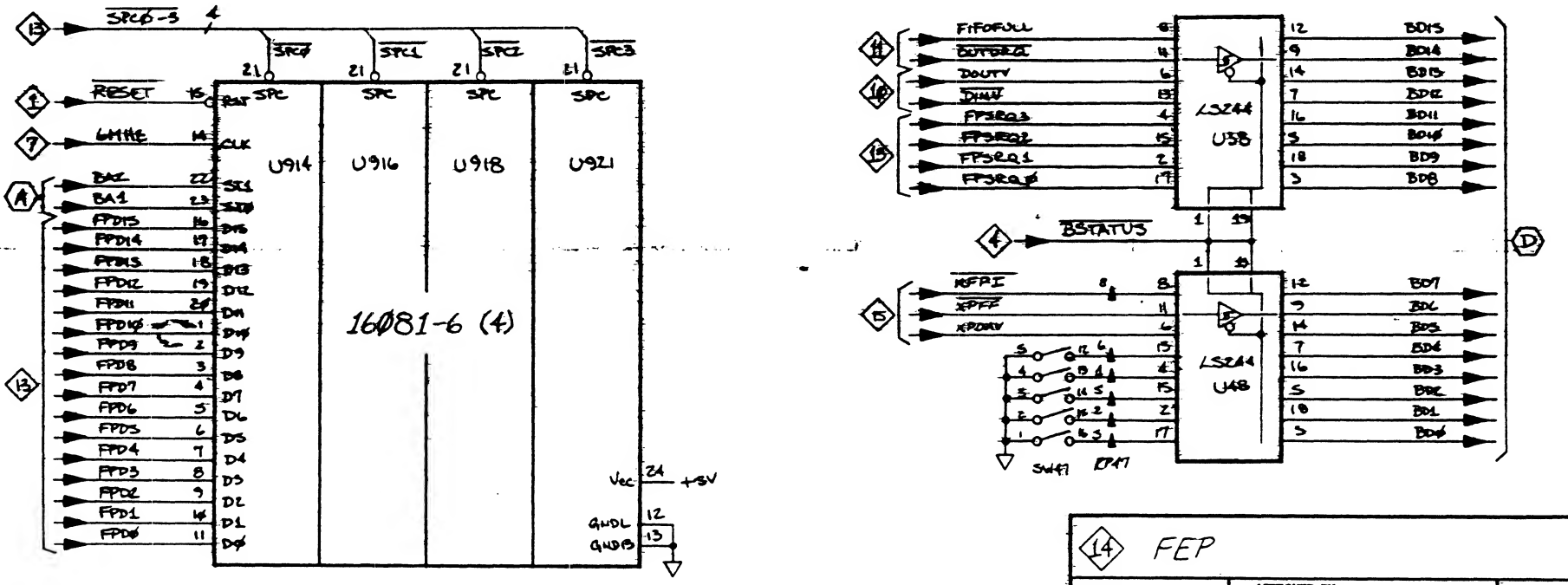
REVISED

DISPLAY CONTROLLER INTFC (FIFO IN)

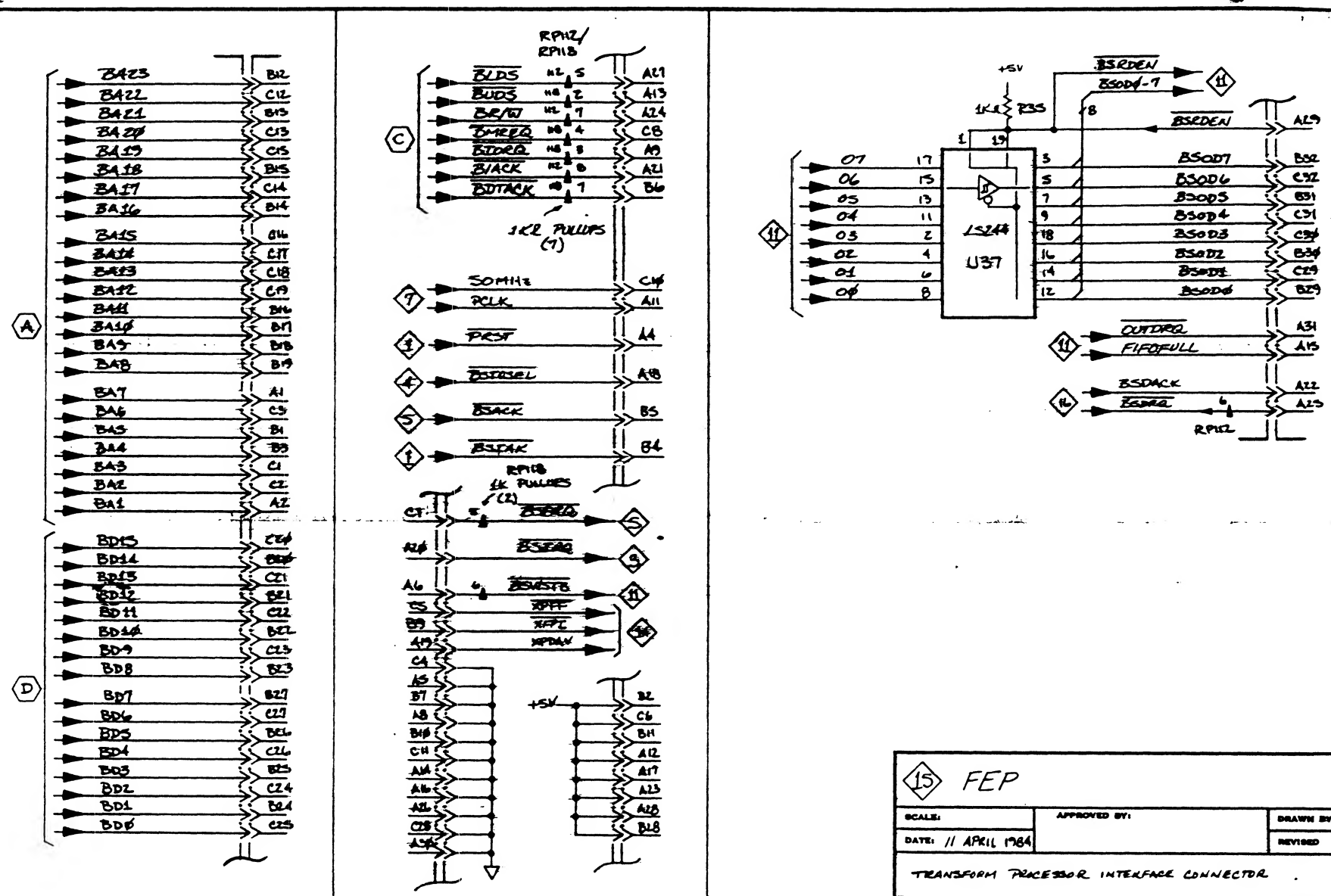
DRAWING NUMBER 11 OF 15


"DMAPAL"
U318
U120
Am 9516A
U218
U117
U321
U320
U118
U319
LS244
LS373
LS245
LS175
DMAACK
TBEN
DBUFFEN
RESET
6MHZ
BDTACK
DMAREQ
DMABEQ
FEP
SCALE:
APPROVED BY:
DRAWN BY HACKIS
DATE: 29 MACCH 84
REVISED
DMA CONTROLLER INTERFACE
DRAWING NUMBER
12 OF
18


PAL16L8
U717
"FPUPAL"
FPUINTEN
BA5
BA4
BA3
BR/W
BLDS
FPUSEL
SWREQ
BSPC0
BSPC1
BSPC2
BSPC3
SPC0
SPC1
SPC2
SPC3
FPUREQ
RBEN
TBEN
1/6 7407 (4)
U817
RPB20
+5V
4.7K (4)
1/2 LS20
SWREQ
6MHz
1/6 LS04
U218
1/6 LS04
U218
U821
U820
1/2 LS109 (4)
P.U.
FPSRQ0
FPSRQ1
FPSRQ2
FPSRQ3
LS373
U718
LS244
U719
LS373
U720
LS244
U721
BD15
BD14
BD13
BD12
BD11
BD10
BD9
BD8
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
FPD15
FPD14
FPD13
FPD12
FPD11
FPD10
FPD9
FPD8
FPD7
FPD6
FPD5
FPD4
FPD3
FPD2
FPD1
FPD0
FPD0-15
BD0-15
FEP
DATE: 9 APRIL 1984
DRAWN BY HARRIS
16081 FPU INTERFACE
DRAWING NUMBER
13 OF



14 FEP	
SCALE:	APPROVED BY:
DATE: 9 APRIL 1984	DRAWN BY HARRIS
	REVISED
16081 FPU's + STATUS REGISTER .	
	DRAWING NUMBER 14 OF



1-20

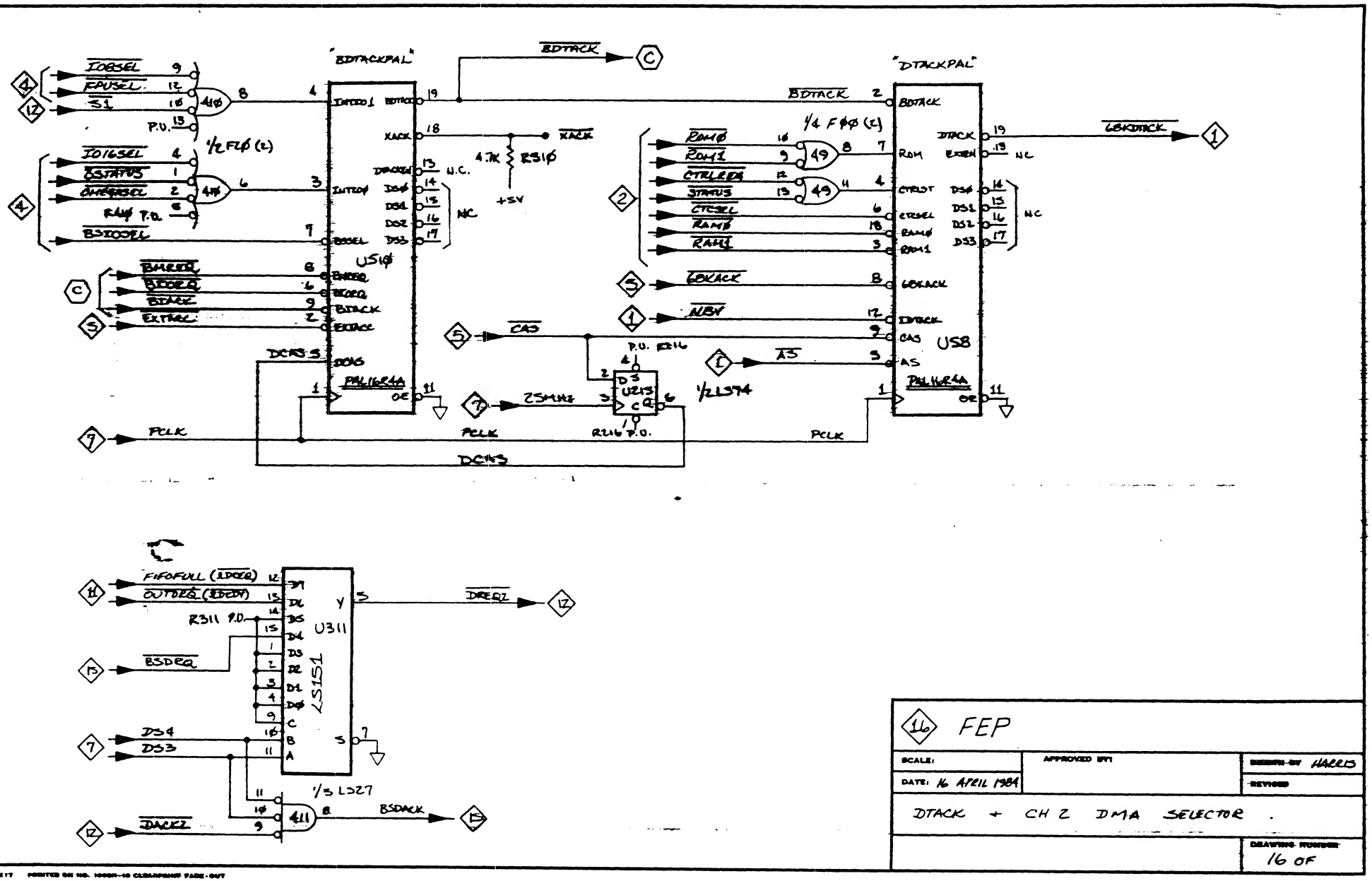
15 FEP

SCALE:	APPROVED BY:	DRAWN BY HARRIS
DATE: 11 APRIL 1984		REVISED

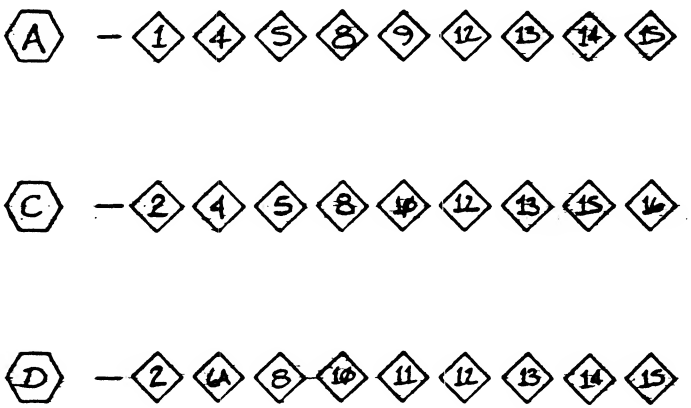
TRANSFORM PROCESSOR INTERFACE CONNECTOR

2

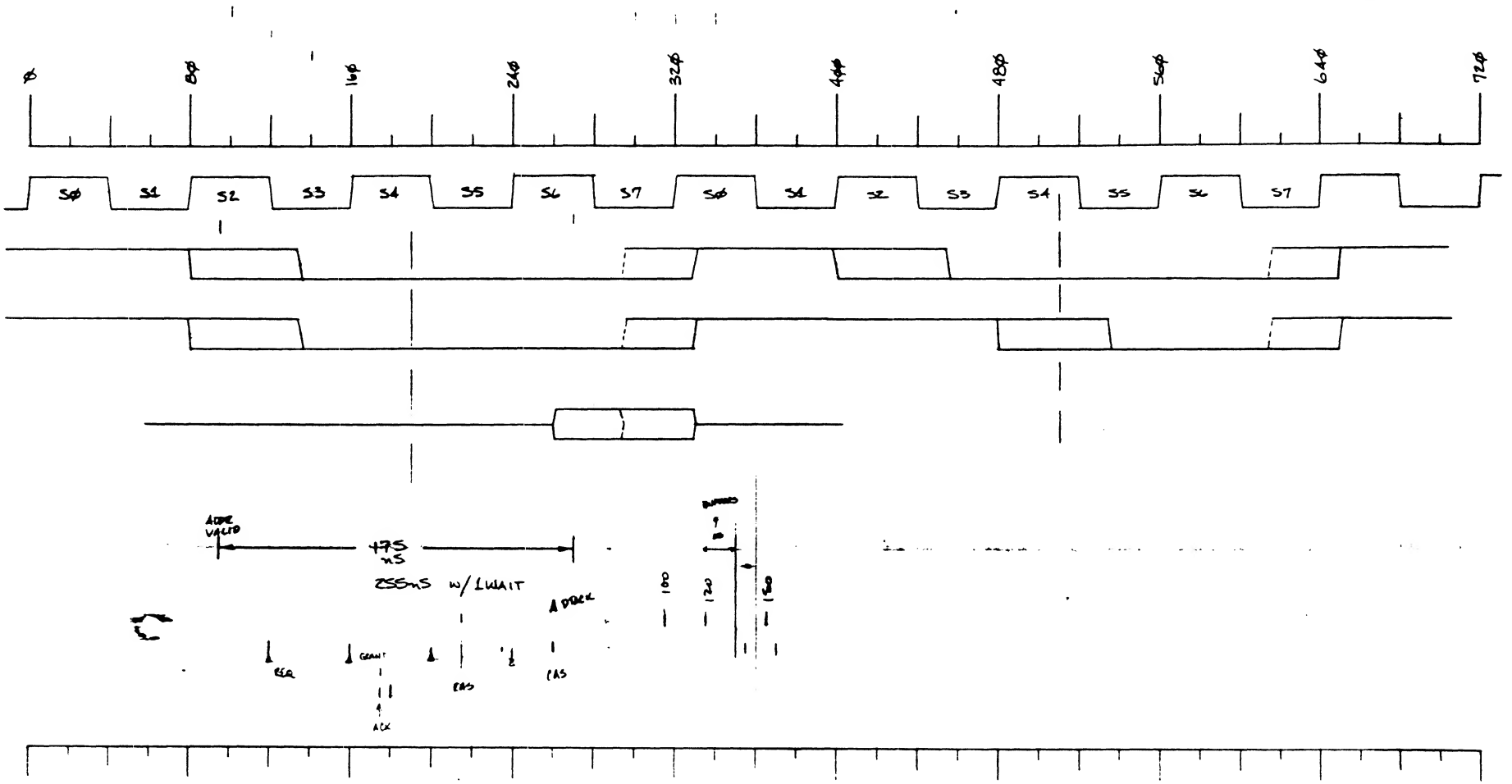
DRAWING NUMBER 15 OF


"BDTACKPAL"
"DTACKPAL"
BDTACK
IOBSEL
RPUSEL
S1
P.U.
1/2 F74 (2)
IO16SEL
BSTATUS
BWRREQ
BRDREQ
BDACK
EXTREQ
DCK53
PAL16R4A
US10
US8
4.7K
R310
+5V
N.C.
NC
CAS
P.U. R316
1/2 LS74
25MHz
PCLK
R316 P.U.
DC53
4/4 F40 (2)
ROM0
ROM1
CTRLREG
STATUS
CTCSEL
RAM0
RAM1
LOKACK
NBW
AS
LOKBTACK
FIFOFULL (IDRQ)
OUTDRQ (BDRQ)
R311 P.U.
U311
LS151
BSDREQ
DS4
DS3
DACK2
1/3 LS27
BSDACK
DREQ2
FEP
SCALE:
APPROVED BY:
DRAWN BY HARRIS
DATE: 16 APRIL 1984
REVISED
DTACK + CH 2 DMA SELECTOR .
DRAWING NUMBER
16 OF

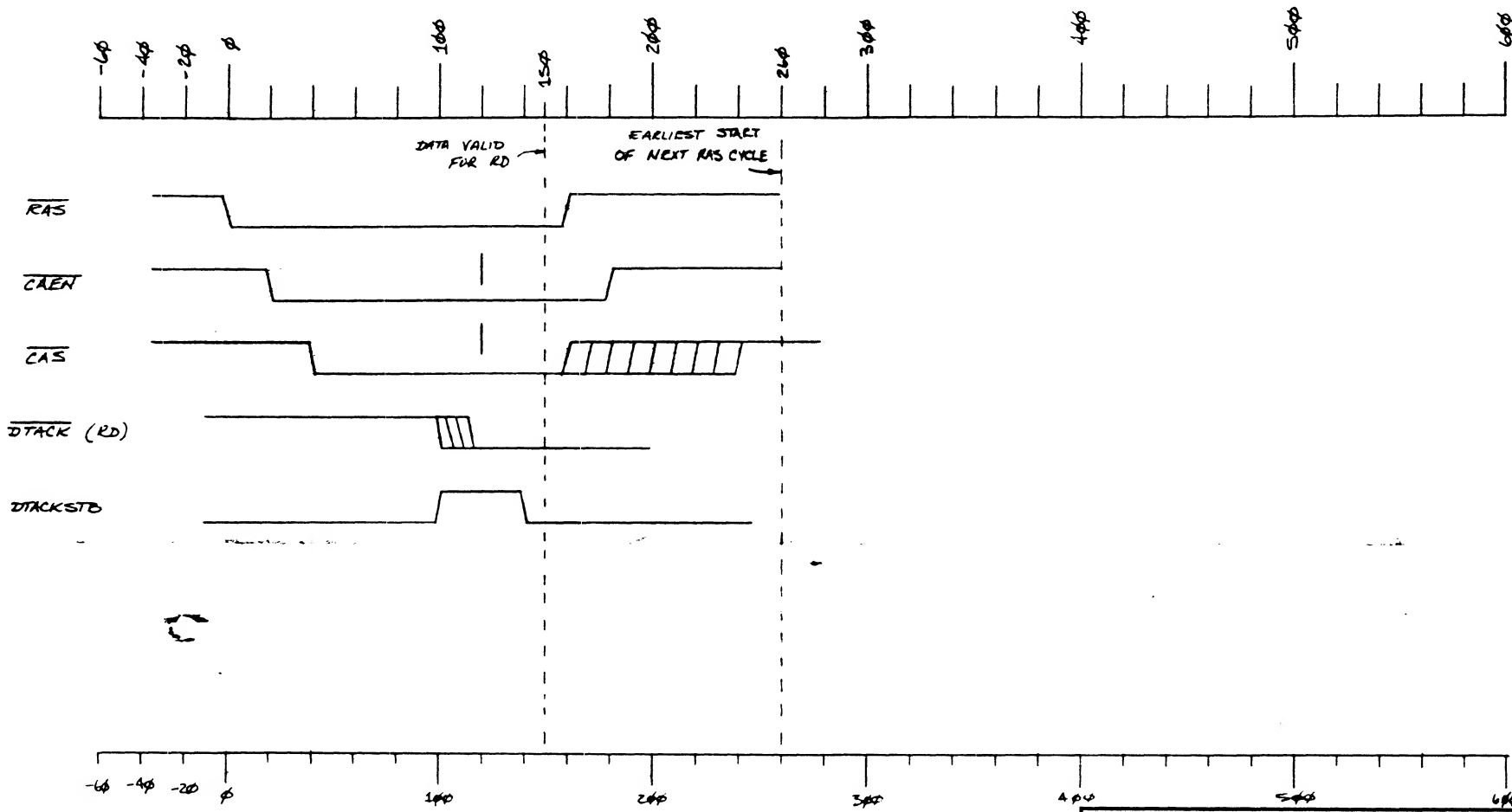
MAIN BUS - ADDRESS, CONTROL + DATA



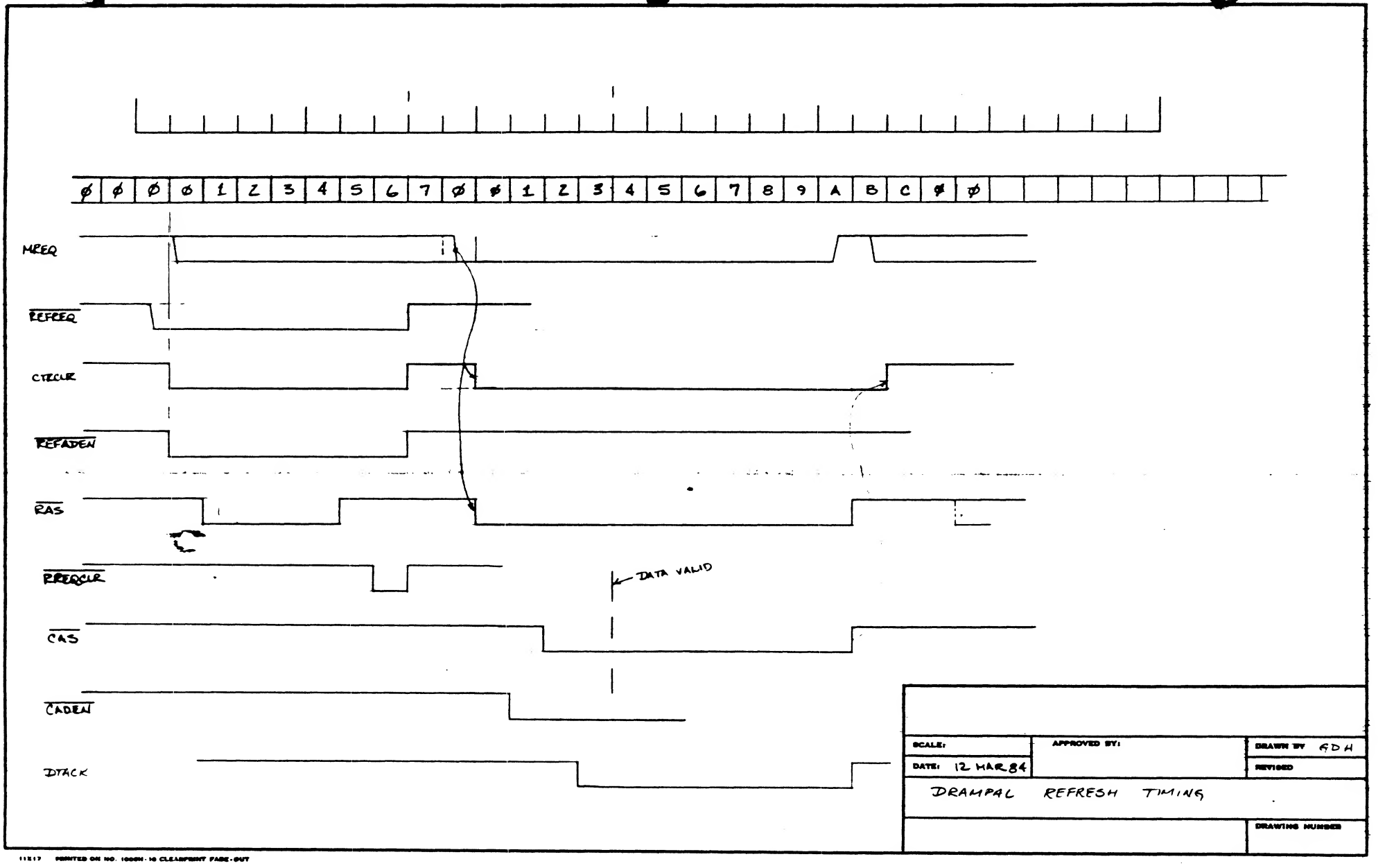
17 FEP		
SCALE:	APPROVED BY:	DRAWN BY HARRIS
DATE: 17 APRIL 1984		REVISED
BUS LEGENDS		
		DRAWING NUMBER 17 OF



SCALE:	APPROVED BY:	DRAWN BY
DATE:		REVISED
		DRAWING NUMBER



SCALE:	APPROVED BY:	DRAWN BY HARRIS
DATE: 1 MAR84		REVISED
150 NS DRAM TIMING W/ 20 NS (50 MHz) TIMING RESOLUTION		
		DRAWING NUMBER



SCALE:	APPROVED BY:	DRAWN BY GDH
DATE: 12 MAR 84		REVISED
DRAMPAL REFRESH TIMING		
		DRAWING NUMBER